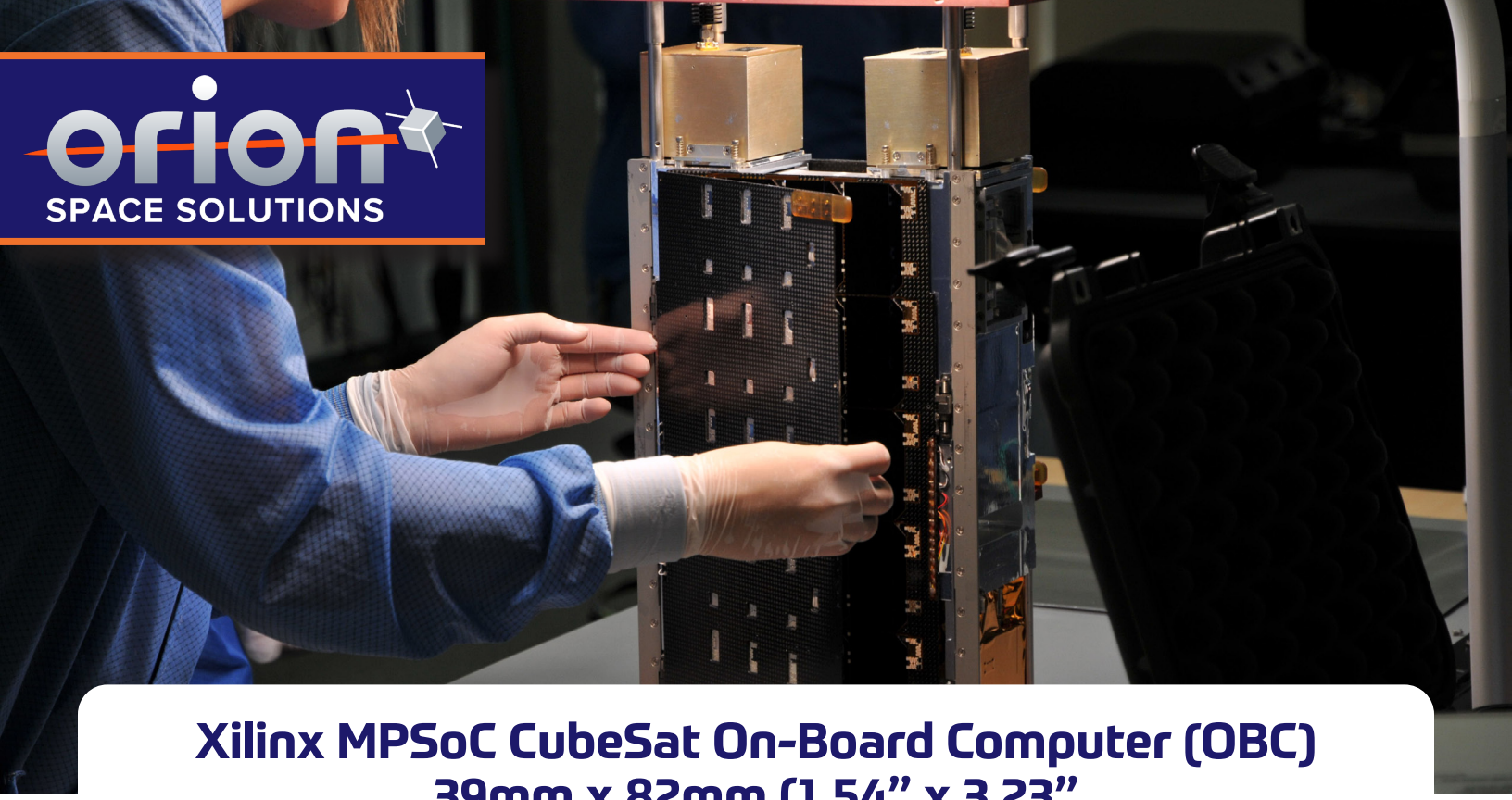


orion SPACE SOLUTIONS

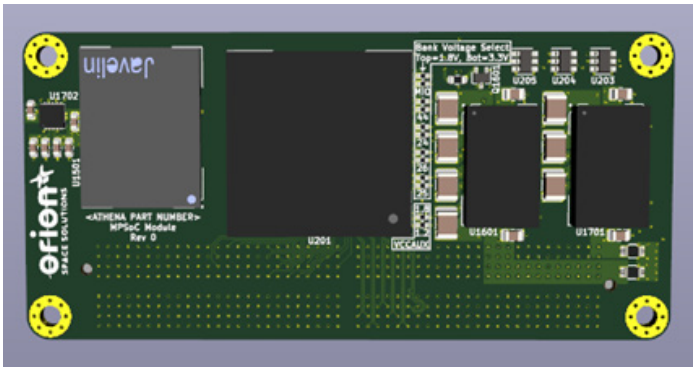
Xilinx MPSoC CubeSat On-Board Computer (OBC)
39mm x 82mm (1.54” x 3.23”

OVERVIEW

The MPSoC OBC is a very small and power-efficient control computer designed for CubeSats. It combines a Xilinx Ultrascale+ MPSoC, 72-bit ECC DDR4 RAM, and point-of-load power regulation onto a single board for easy integration into multiple applications.

All configuration, I/O, and current monitors are broken out to the 400-pin expansion header, allowing customization to take place on the carrier board. This allows for application-specific boot and data storage devices, as well as remote monitoring of critical subsystems (for example, using a rad-hard MCU for voltage/current/SEU monitoring and watchdog).

The MPSoC architecture features a quad-core 1.2 GHz ARM A53 CPU which can be configured to run Linux, bare-metal applications, or a combination of the two. The CPU is mated to a 100-250K logic cell



PROGRAM HIGHLIGHTS

- Supports any ZU2EG to ZU5EG MPSoC in the SFVC784 package
  - » *Quad-core 1.2 GHZ ARM A53*
  - » *100–250K logic cell FGPA linked to CPU through high-speed DMA*
- Supports defense-grade XQ parts with LVAUX mode and remote system reset for SEU mitigation
- Current monitors and power-good feedback routed to I/O header for remote monitoring
- 4–8 GB 72-bit ECC DDR4
  - » *Industrial or military temperature grade*
  - » *Rad-hard Teledyne DDR4 available in same package*
- 4.5–5.5V input, current draw around 0.5–1A depending on FPGA/CPU load
- 78 CPU-controlled MIO I/O (1.8 or 3.3V)
  - » *Supports UART, SPI, I2C, GbE, QSPI Flash, SD, eMMC*
- 58 FPGA-controlled single-ended I/O (1.8 or 3.3V)
- 39 FPGA-controlled LVDS pairs (can be substituted for GTY transceivers as needed)

KEY BENEFITS

- Small, power-efficient control computer designed for CubeSats
- Easy integration into multiple applications

FPGA through a high-speed DMA. This CPU+FPGA combination allows the ultimate in flexibility. Tasks and interfaces that require high speed or low latency can be developed on the FPGA, while tasks that benefit from the ease of programming in high level languages can be developed on the CPU, and the high-speed DMA linking them allows the user to transfer messages or data across with minimal effort. The end result is that a single high-level application on the CPU is able to easily communicate with and route data between subsystems over multiple GbE and as many UART, RS422, SPI, I2C, spacewire, parallel CMOS/LVDS, and other low-level interfaces as can fit in the available FPGA I/O. FPGA firmware updates are as simple as uploading a new bitstream file into the Linux filesystem.